Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A communication method comprising:

receiving data from a first plurality of data lines, each data line providing data at a predetermined rate;

serializing the received data;

providing the serialized data over a link;

deserializing the serialized data to create deserialized data using a clock signal having a phase determined based on edges in the serialized data that occur at least once every other cycle of the clock signal and that are generated by complimenting a first data line of the first plurality of data lines to obtain a second data line of the first plurality of data lines; and

providing the deserialized data to a second plurality of data lines corresponding to the first plurality of data lines.

2. (currently amended) The method of claim 1, wherein the act of serializing includes:

multiplexing data from [[a]] the first and [[a]] the second of the first plurality of data lines onto a single data line clocked at a multiple of the predetermined rate.

3. (canceled)

4. (canceled)

5. (original) The method of claim 1, wherein the link includes an optical fiber for carrying the serialized data.

6. (original) The method of claim 1, further including:

detecting a predetermined pattern in the deserialized data; and

aligning the deserialized data with other data based on the detected pattern.

7. (original) The method of claim 1, wherein the act of providing serialized data includes:

transmitting the serialized data asynchronously through the link.

8. (original) A communication system comprising:

a plurality of input data signal lines carrying data transmitted synchronously with a first clock signal running at a predetermined frequency;

a plurality of multiplexers each configured to receive a subset of the plurality of input data signal lines and to combine data received on the subset of data signal lines into combined signals, at least one of the plurality of multiplexers receiving, as the subset of the plurality of data signal lines, a first of the plurality of data signal lines and a complement of the first of the plurality of data signal lines;

a transmission system coupled to the plurality of multiplexers and configured to transmit the combined signals;

a plurality of demultiplexers configured to convert the combined signals to data signals on a plurality of output data signal lines based on a second clock signal; and

a clock recovery circuit configured to provide the demultiplexers with the second clock signal based on the combined signals.

9. (original) The communication system of claim 8, further comprising:

an inverter connected to receive the first of the plurality of data signal lines and to output the complement of the first data signal line.

10. (original) The communication system of claim 8, further comprising:

a transmitter configured to receive data from the plurality of input data signal lines and to transmit the data to the plurality of multiplexers, the transmitter periodically inserting a predetermined pattern into the data; and

a receiver configured to receive data from the plurality of data signal lines from the demultiplexers and to identify the predetermined pattern in the received data, the receiver aligning and correcting bit transpositions of the received data based on the predetermined pattern.

11. (original) The communication system of claim 8, wherein each of the plurality of multiplexers combines the data signal lines into combined signals having a data transmission frequency which is a multiple of the predetermined frequency.

12. (original) The communication system of claim 8, wherein the transmission system further includes:

transmitters connected to outputs of the multiplexers, the transmitters receiving the combined signals and transmitting the combined signals; and

receivers configured to receive the signals transmitted by the transmitters.

13. (original) A network device for transmitting information over a link, the network device comprising:

a first multiplexer connected to a plurality of data lines each having an output, the first multiplexer combining data signals from the plurality of data lines;

a second multiplexer including a first input connected to the plurality of data lines, a second input connected to a line carrying a complement of data received by the first input, and an output, the second multiplexer combining data signals from the first and second inputs; and

transmitters connected to the outputs of the first and second multiplexers, the transmitters receiving the combined data signals from the first and second multiplexers and transmitting the combined data signals to a link.

14. (original) The network device of claim 13, further comprising:

a circuit for receiving data for the plurality of data lines synchronously with a first clock signal running at a predetermined frequency.

15. (original) The network device of claim 13, further comprising:

a circuit for transmitting a predetermined pattern on the plurality of data lines.

16. (original) The network device of claim 13, wherein the network device is a router.

17. (original) The network device of claim 13, wherein the line carrying a complement comprises:

an inverter outputting the complement of the data received by the first input of the second multiplexer.

18. (original) A network device for receiving information, the network device comprising:

receivers connected to a link, the receivers receiving the information from the link and converting the information to first data signals and transmitting the data signals on data lines;

a first demultiplexer connected to the data lines, the first demultiplexer converting the first data signals into second and third data signals, and outputting

the second data signal based on a clock signal and outputting the third data signal based on the clock signal, the third data signal being a complement of the second data signal; and

a clock recovery circuit connected to the data lines, the clock recovery circuit generating the clock signal based on a detection of repeating edges in the first data signals and providing the clock signal to the first demultiplexer.

19. (original) The network device of claim 18, further comprising:

a second demultiplexer receiving the clock signal from the clock recovery circuit and outputting demultiplexed data signals.

20. (original) The network device of claim 19, further comprising:

a receiver connected to receive data signals from at least the first or second demultiplexer, the receiver identifying a predetermined pattern in the received data signals and aligning data bits and correcting bit transpositions in the data signals based on the predetermined pattern.

21. (original) The network device of claim 18, wherein the network device is a router.

22. (currently amended) A communication system comprising:

means for receiving data from a first plurality of data lines, each data line providing data at a predetermined rate;

means for serializing the received data;

a circuit for transmitting the serialized data;

means for generating a clock signal based on the serialized data by synchronizing a phase of the clock signal based on edges in the serialized data that occur at least once every other cycle of the clock signal and that are generated by complimenting a first data line of the first plurality of data lines to obtain a second data line of the first plurality of data lines;

means for deserializing the serialized data using the clock signal to create deserialized data; and

means for providing the deserialized data to a second plurality of data lines.

23. (currently amended) The communication system of claim 22, wherein the means for serializing further comprises:

means for multiplexing data from [[a]] the first and [[a]] the second of the plurality of data lines onto a single data line at a rate different from the predetermined rate.

24. (canceled)

25. (canceled)

26. (original) The communication system of claim 22, further comprising:

means for aligning the phase of a clock signal based on the serialized data.

27. (original) The communication system of claim 22, further comprising:

an optical link for transmitting the serialized data.

28. (original) The communication system of claim 22, further comprising:

means for detecting a predetermined pattern in the deserialized data; and

means for aligning data from the data lines based on the detected pattern.

29. (previously presented) The communication system of claim 22, wherein data on the first plurality of data lines is provided synchronously with a second clock signal and wherein the serialized data is provided asynchronously.

30. (previously presented) A network device for transmitting information over a link, the network device comprising:

a component configured to receive data signals at a predetermined rate and to output the data signals to a plurality of data lines, the component periodically inserting a predetermined pattern into the received data signals;

a plurality of multiplexers each connected to a subset of the plurality of data lines, the plurality of multiplexers combining data signals from the subset of the data lines;

an additional multiplexer including a first input connected to the plurality of data lines and a second input connected to a complement of the first input, the additional multiplexer combining data signals from the first and second inputs and generating an output; and

transmitters connected to the plurality of multiplexers and the additional multiplexer, the transmitters receiving the combined data signals from the multiplexers and transmitting the combined data signals over the link.

31. (original) The network device of claim 30, wherein the link is an optical link.

32. (canceled)

33. (previously presented) A network device for receiving information, the network device comprising:

receivers connected to a link, the receivers receiving the information from the link and converting the information to first data signals and transmitting the data signals on data lines;

a first demultiplexer connected to the data lines, the demultiplexer converting the first data signals into second and third data signals, and outputting

the second data signal based on a clock signal and outputting the third data signal based on the clock signal;

a second demultiplexer connected to the data lines, the second demultiplexer converting the first data signals into fourth and fifth data signals, the fourth and fifth data signals being complements of one another;

a clock recovery circuit connected to the data lines, the clock recovery circuit generating the clock signal based on the first data signals and providing the clock signal to the first demultiplexer; and

a receiver connected to receive the second and third data signals, the receiver analyzing the second and third data signals for the presence of a predetermined pattern, the receiver using the predetermined pattern to align bits and correct transposed bits in the second and third data signals.

34. (canceled)

35. (original) The network device of claim 33, wherein the network device is a router.